

Fig 1A

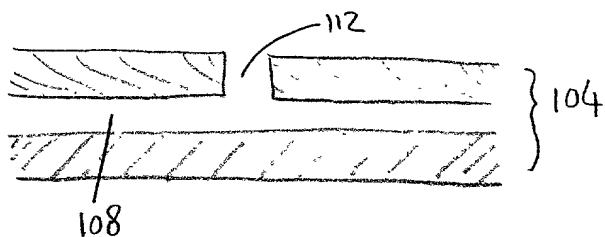


Fig 1B

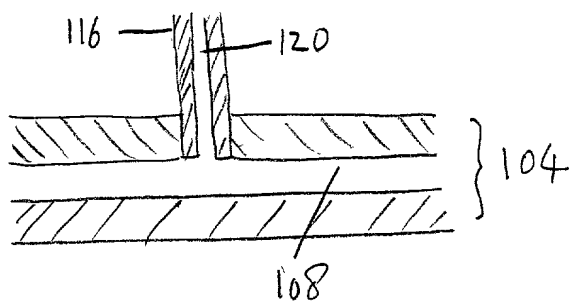


Fig 1C

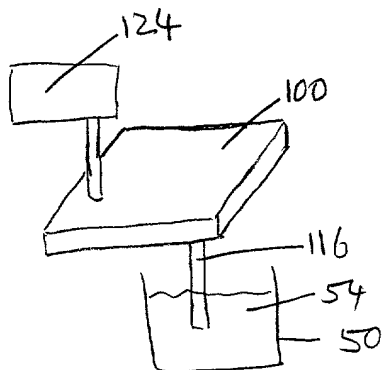


Fig 2A

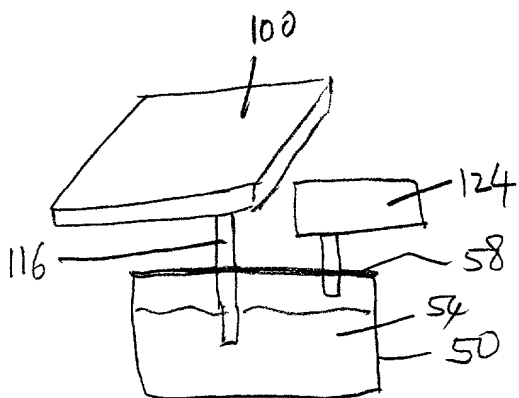


Fig 2B

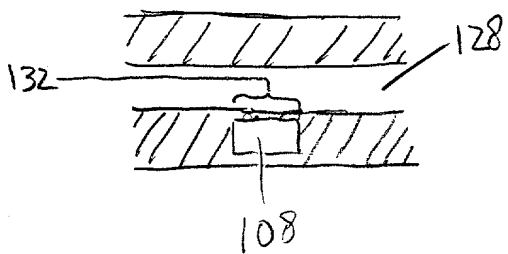


Fig 3A

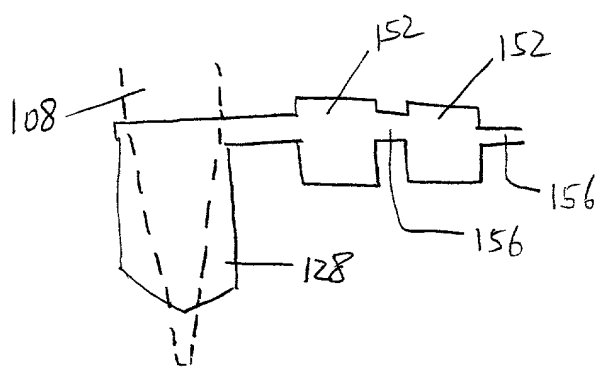


Fig 3B

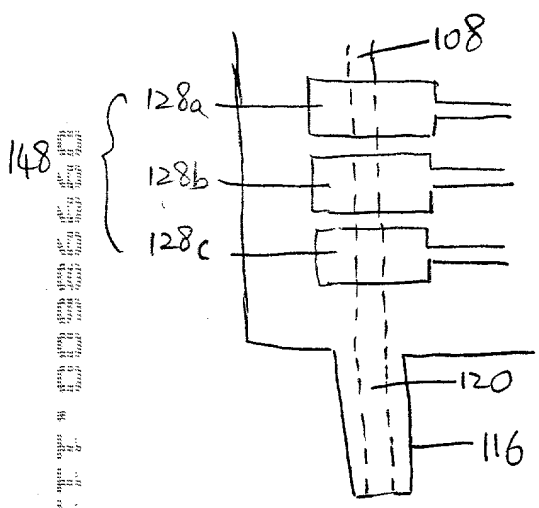


Fig 3C

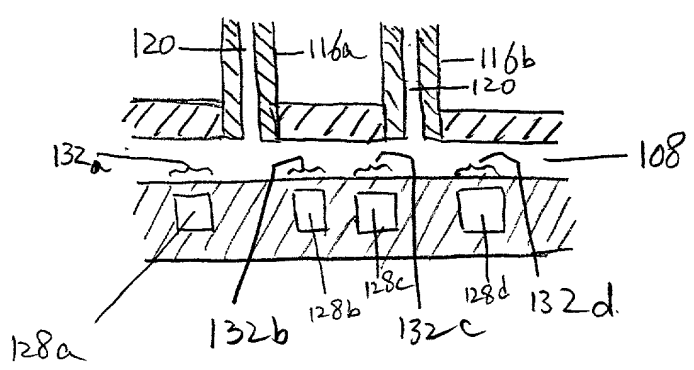


Fig 3D

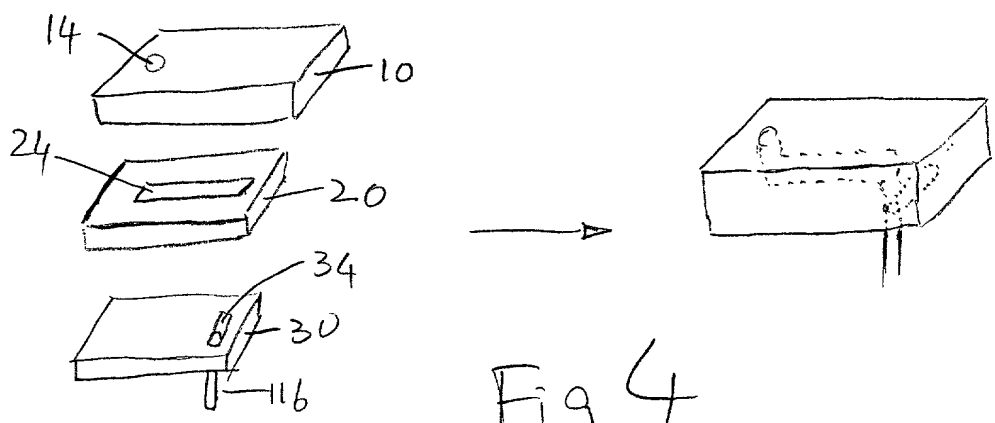


Fig 4

Fig. 5A is a schematic diagram of a semiconductor device in a first stage of a manufacturing process. The device includes a substrate 100, a gate stack 104, and a source/drain region 108. A first conductive layer 112 is formed on the substrate 100, and a second conductive layer 116 is formed on the first conductive layer 112. The gate stack 104 is formed on the second conductive layer 116. The source/drain region 108 is formed in the substrate 100. The first conductive layer 112 is formed by a first conductive material, and the second conductive layer 116 is formed by a second conductive material. The gate stack 104 is formed by a gate dielectric layer and a gate conductive layer. The source/drain region 108 is formed by a source/drain conductive material.

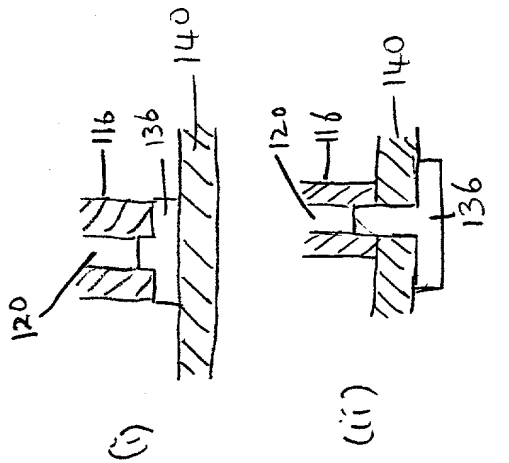


Fig 5A

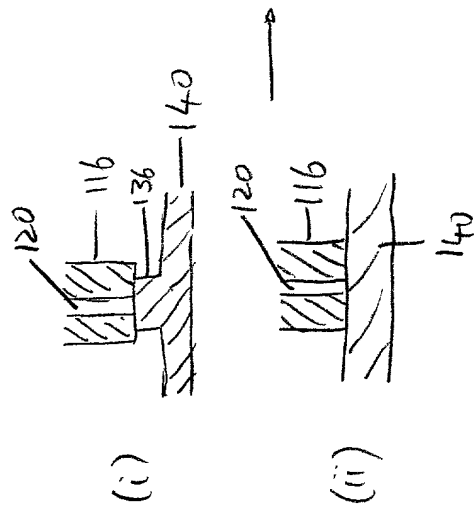


Fig 5B

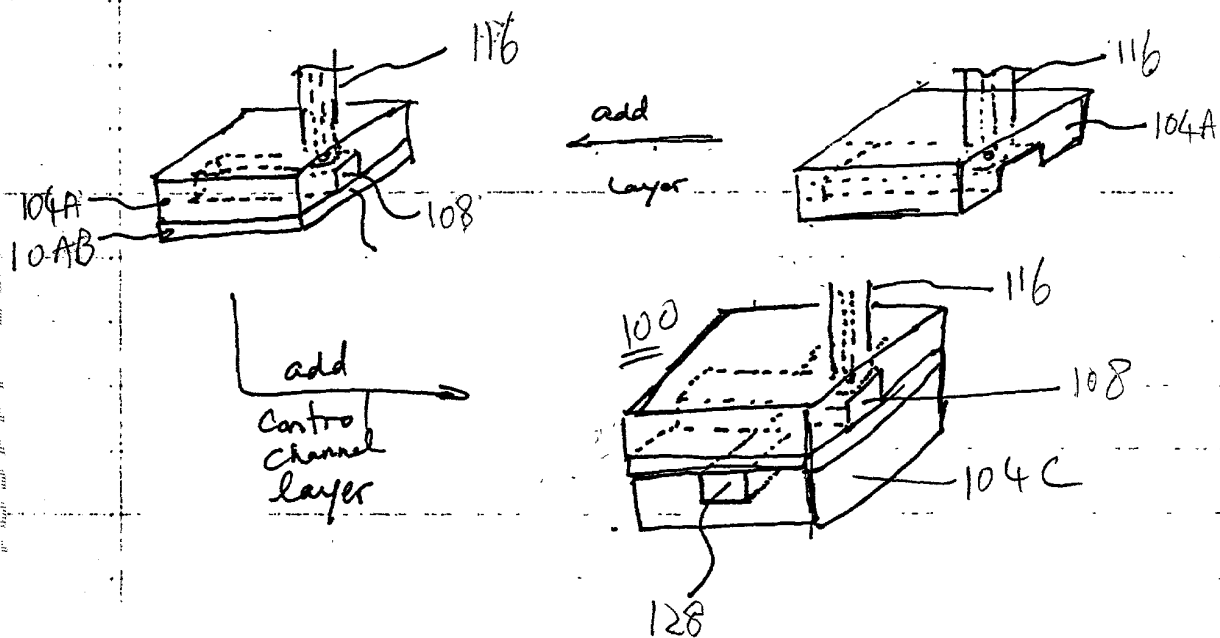
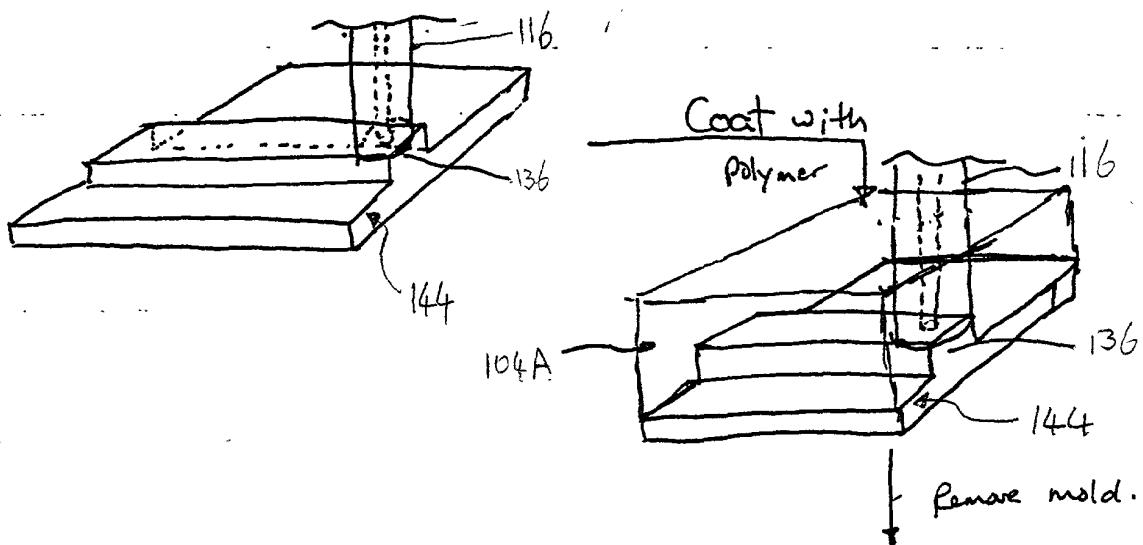


Figure 5C

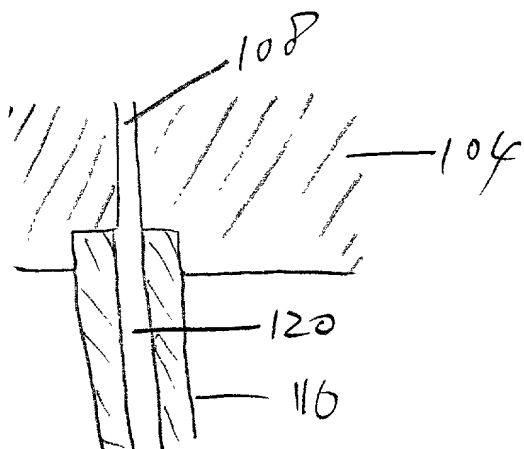
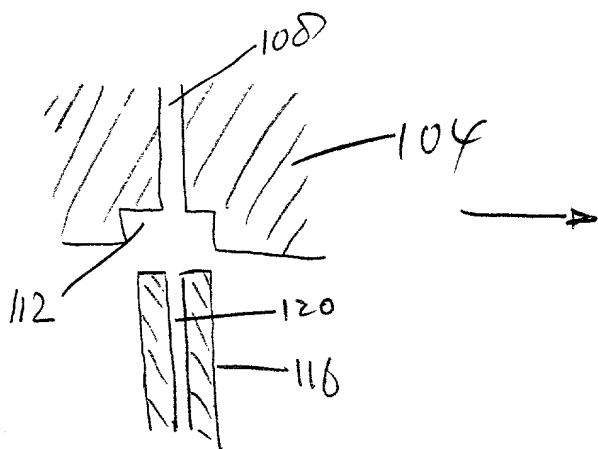
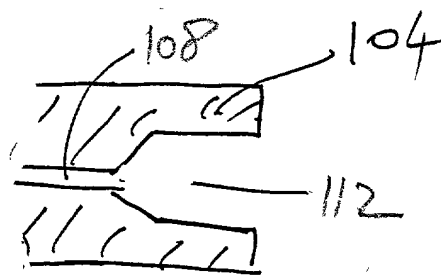
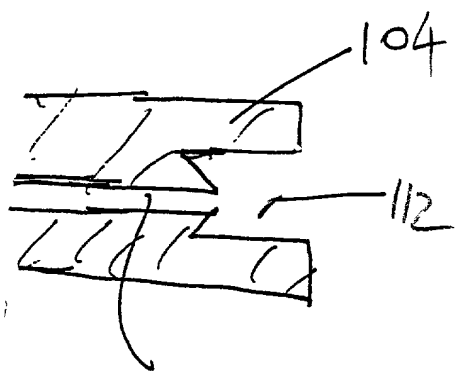


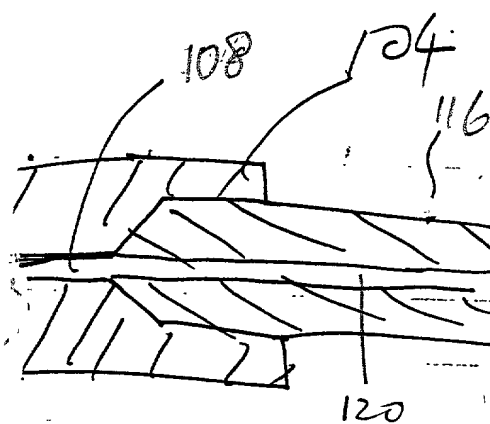
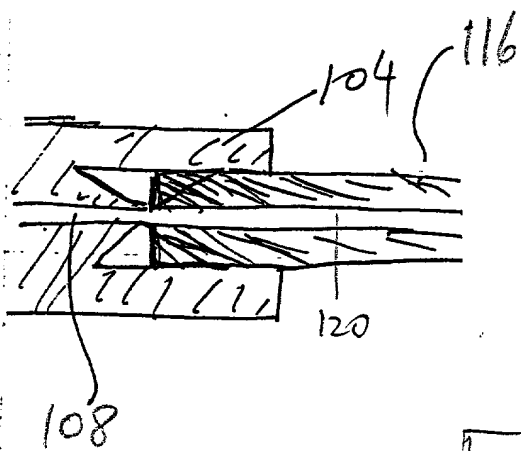
Fig 6A

108
 104
 112
 120
 116



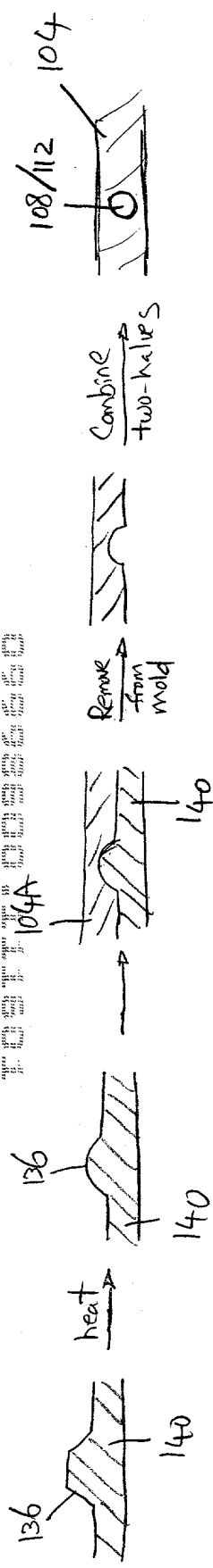
108

Fig 6B



108

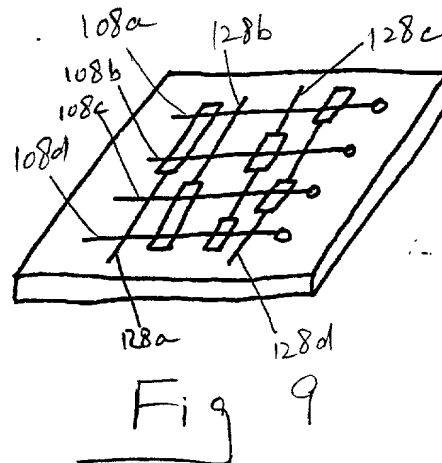
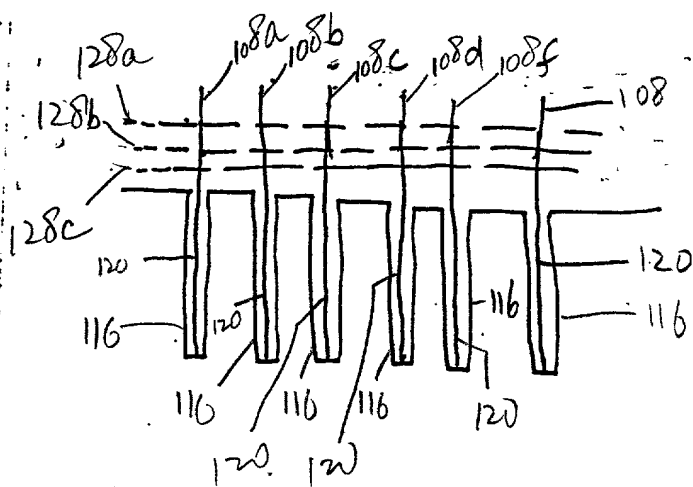
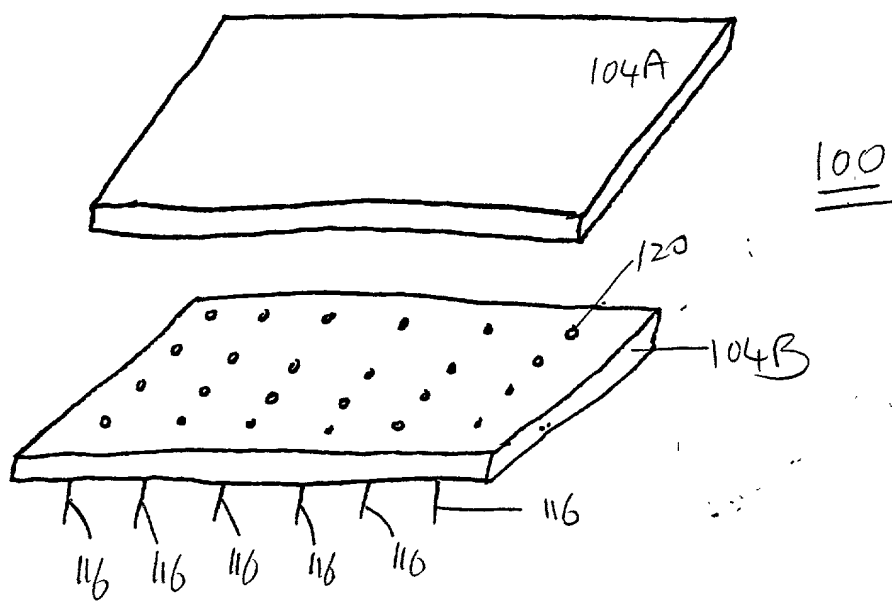
Fig 6C



Combine
two halves

Remove
from
mold

Fig 7



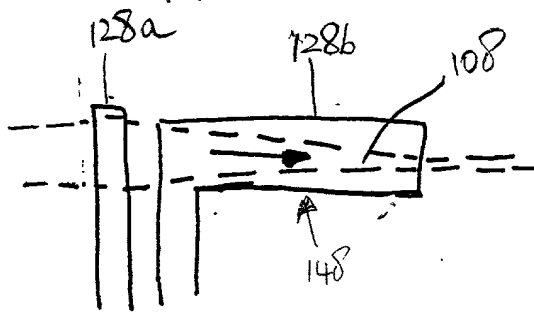


Fig 10A

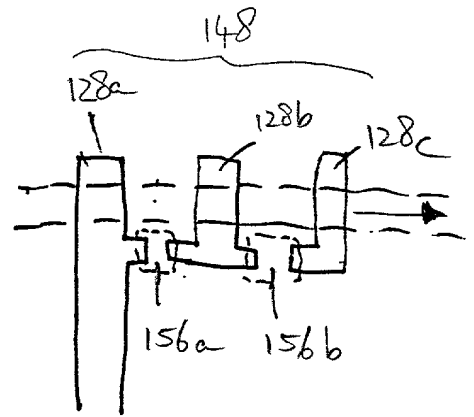


Fig 10E

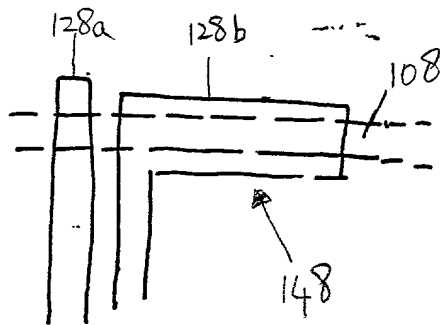


Fig 10B

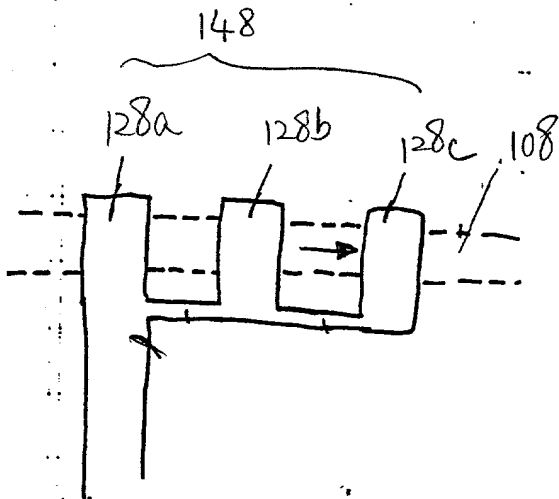


Fig 10C

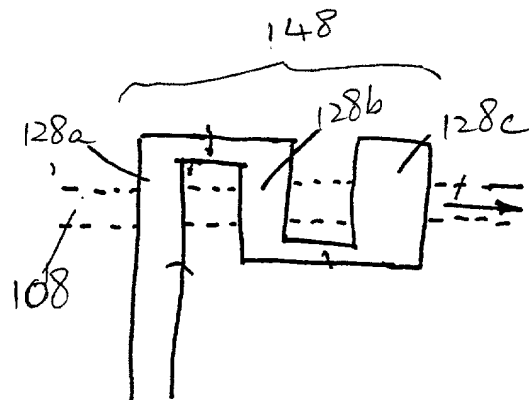


Fig 10D

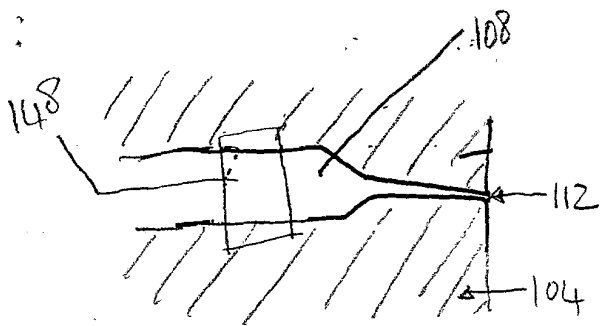


Fig 11B

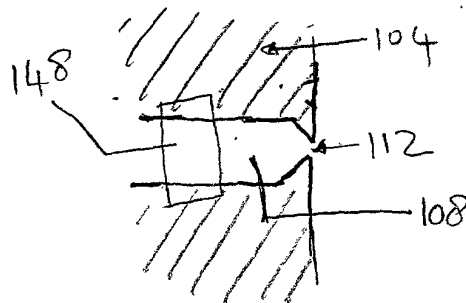


Fig 11C

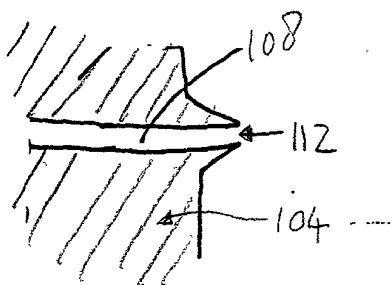


Fig 11A

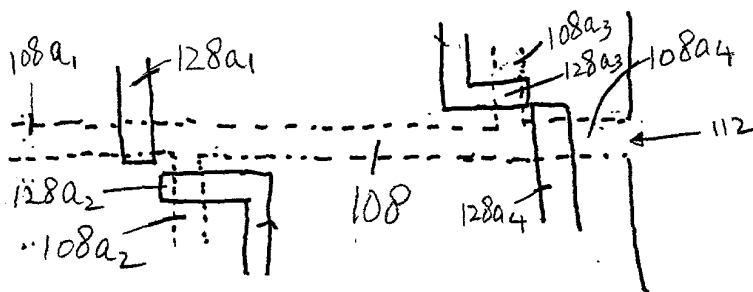


Fig 12A

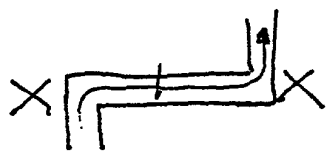


Fig 12B

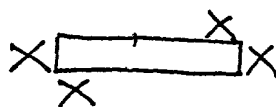


Fig 12C

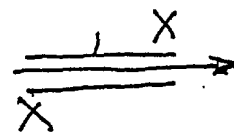
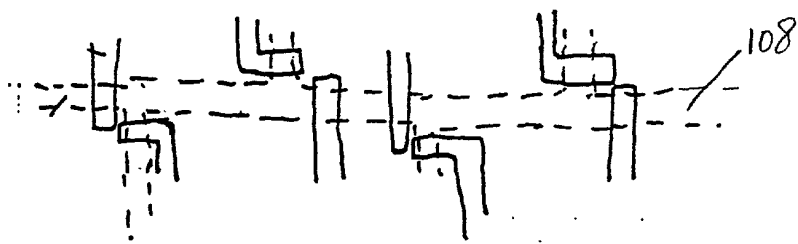


Fig 12D



12E

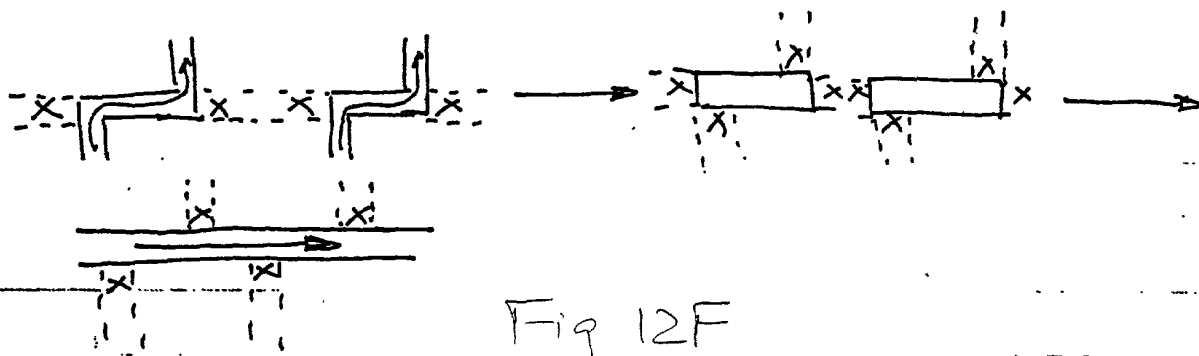


Fig 12F

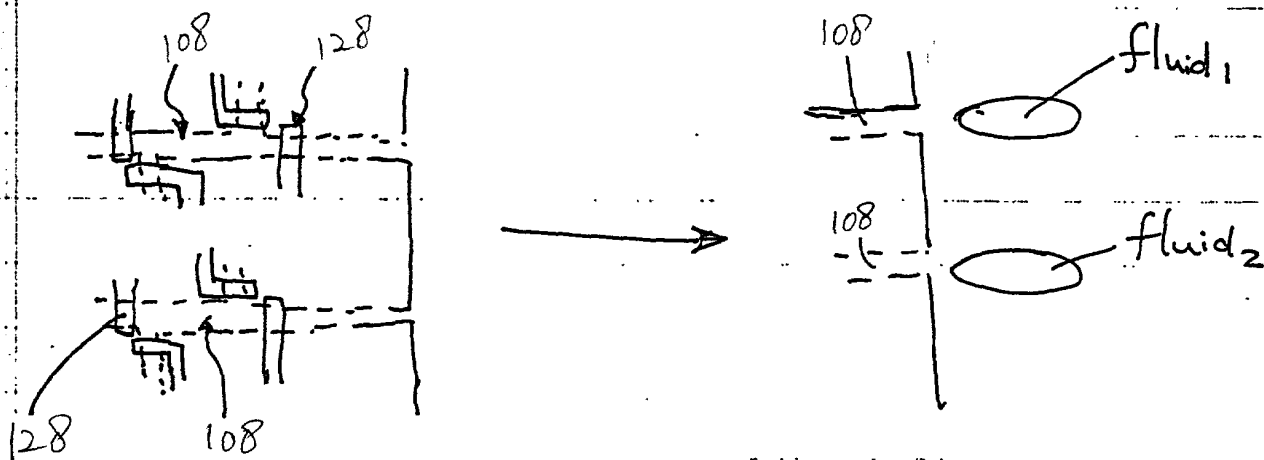


Fig 12G

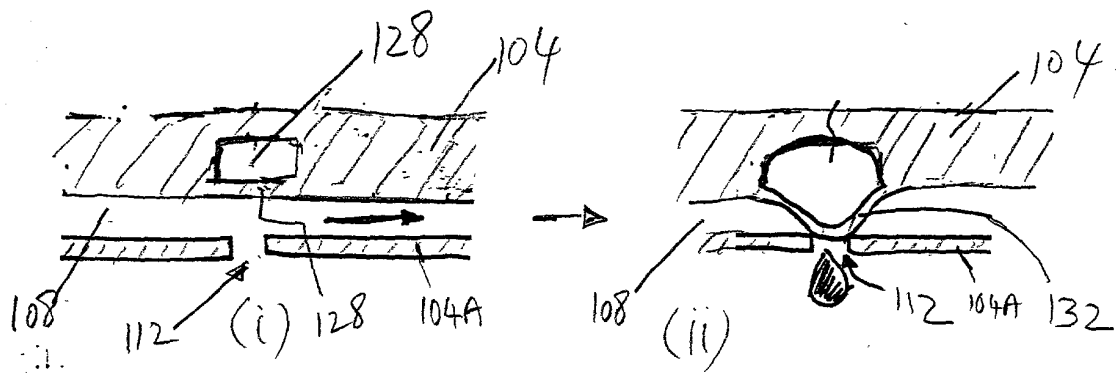


Fig 13A

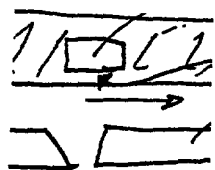


Fig 13B

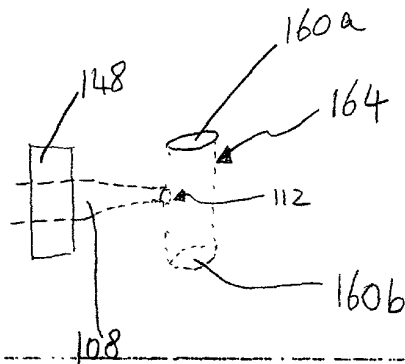


Fig 15A

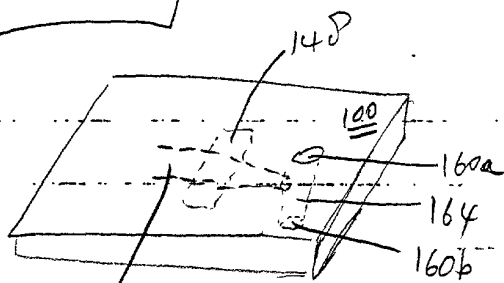


Fig 15B

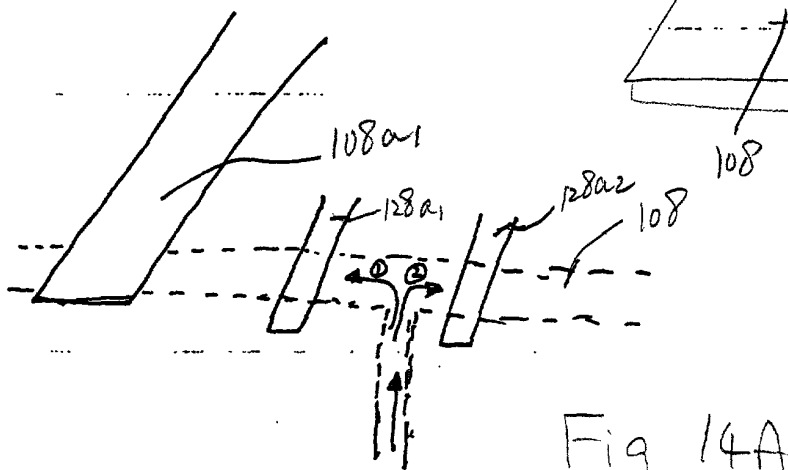


Fig 14A

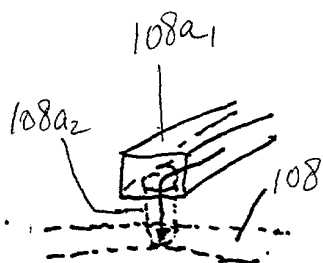


Fig 14B

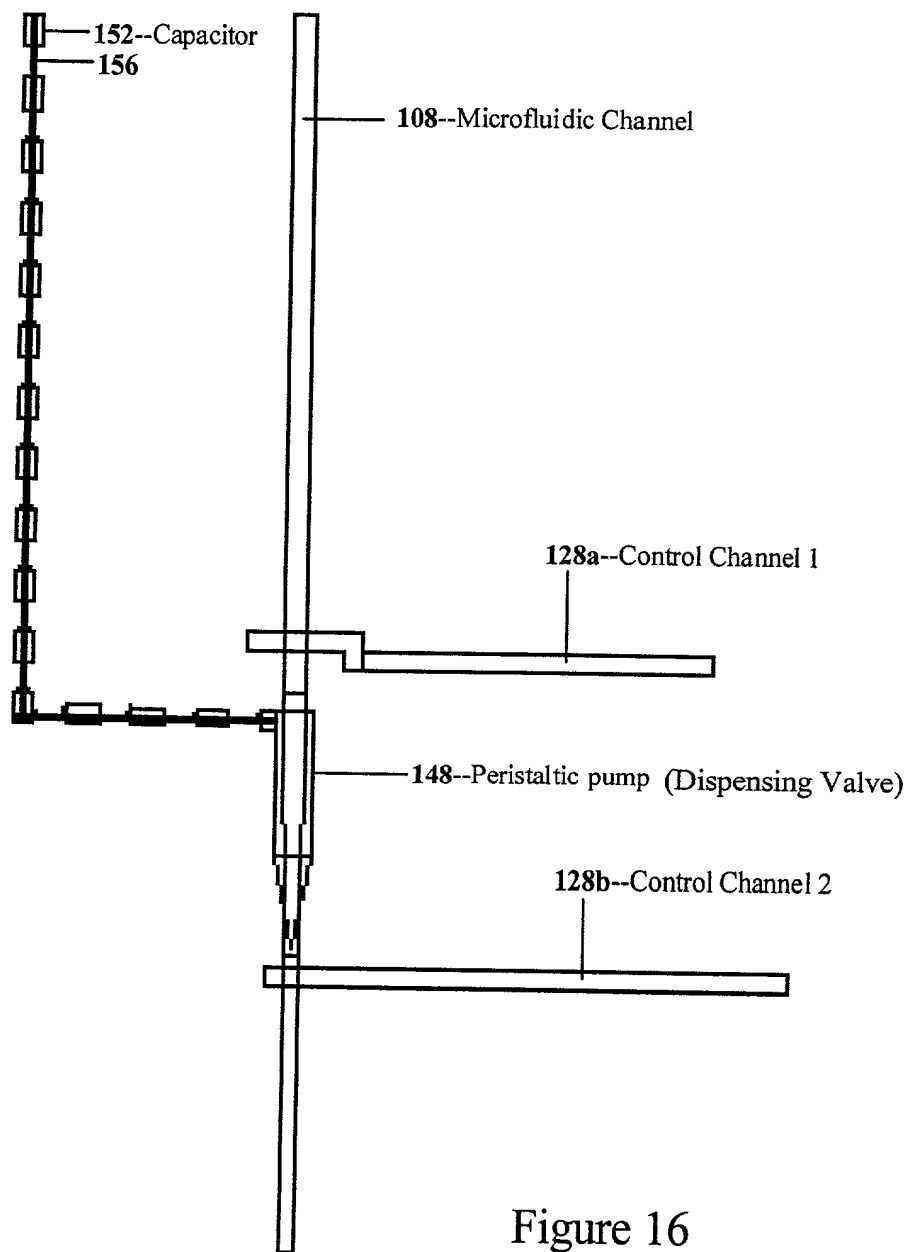


Figure 16

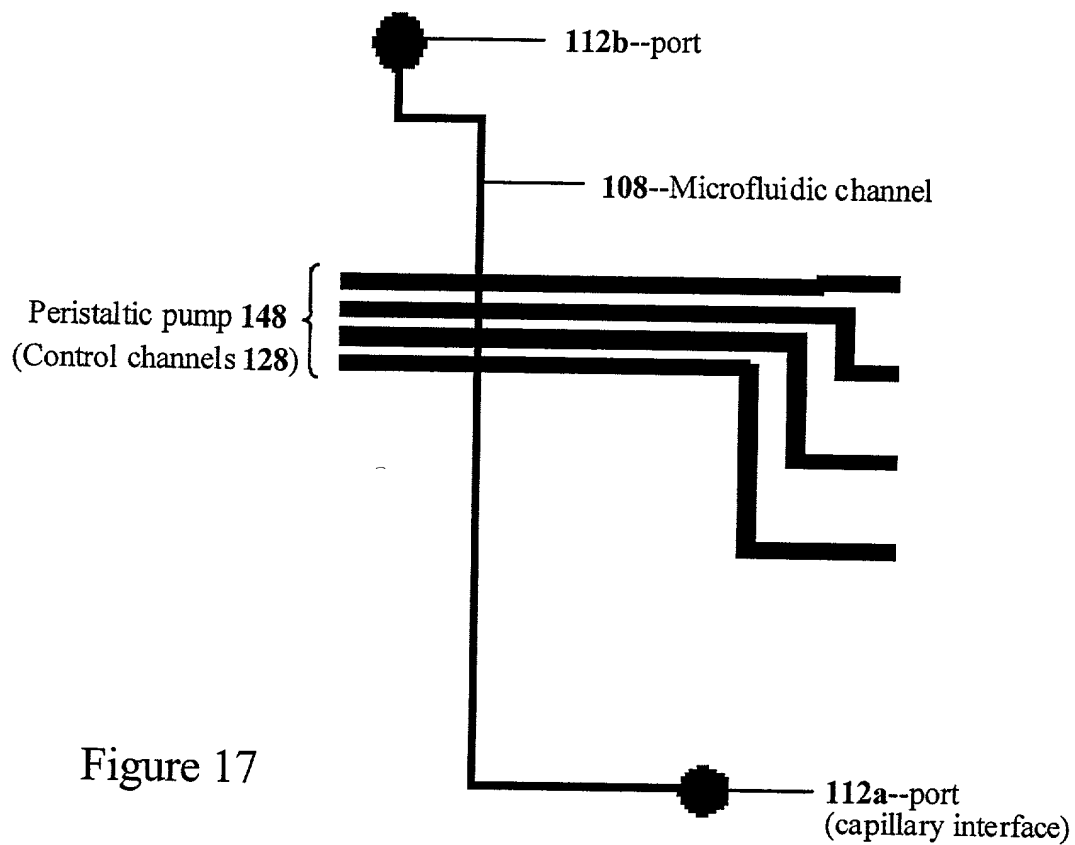


Figure 17

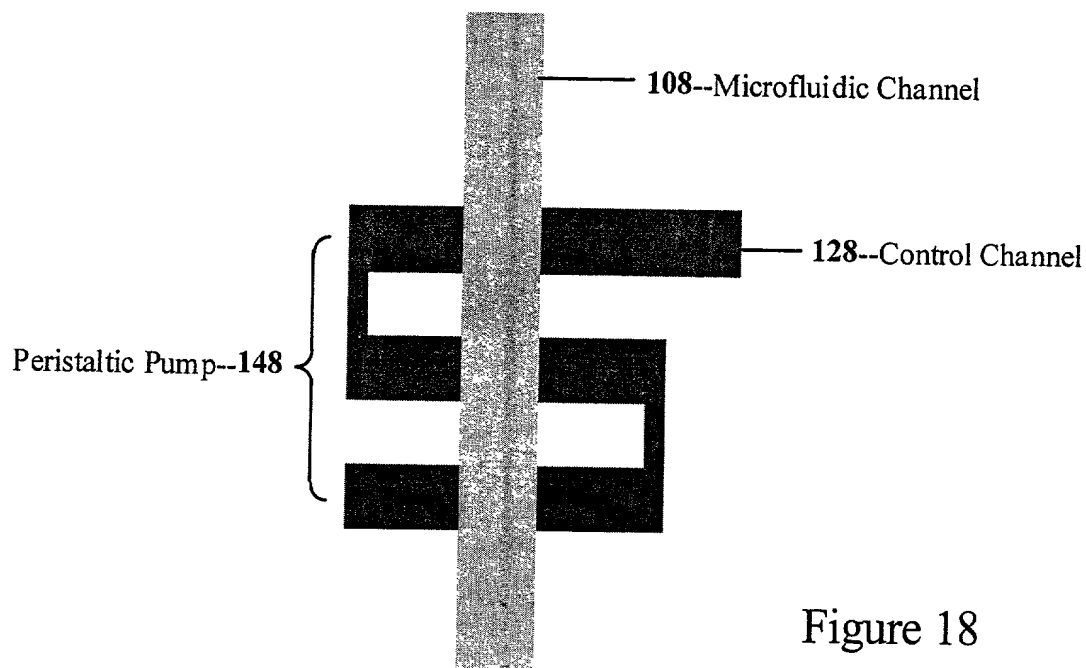


Figure 18

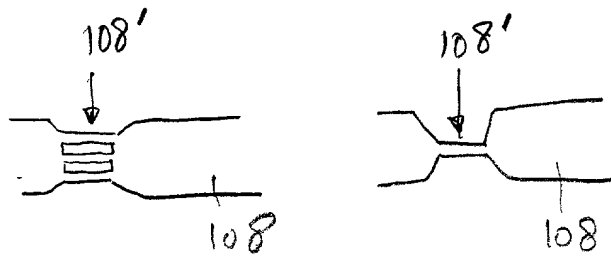


Fig 19

FIG. 20A

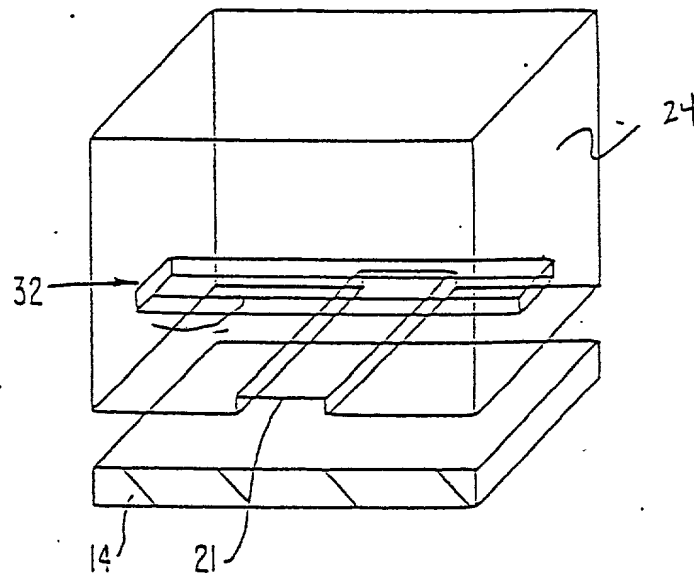
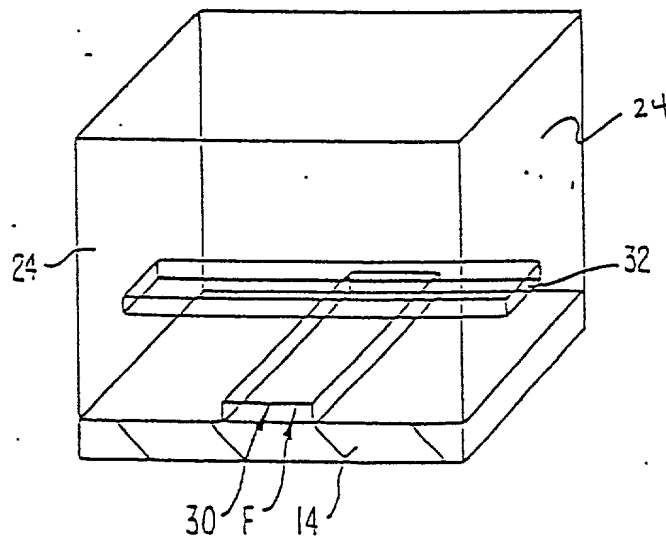


FIG. 20B



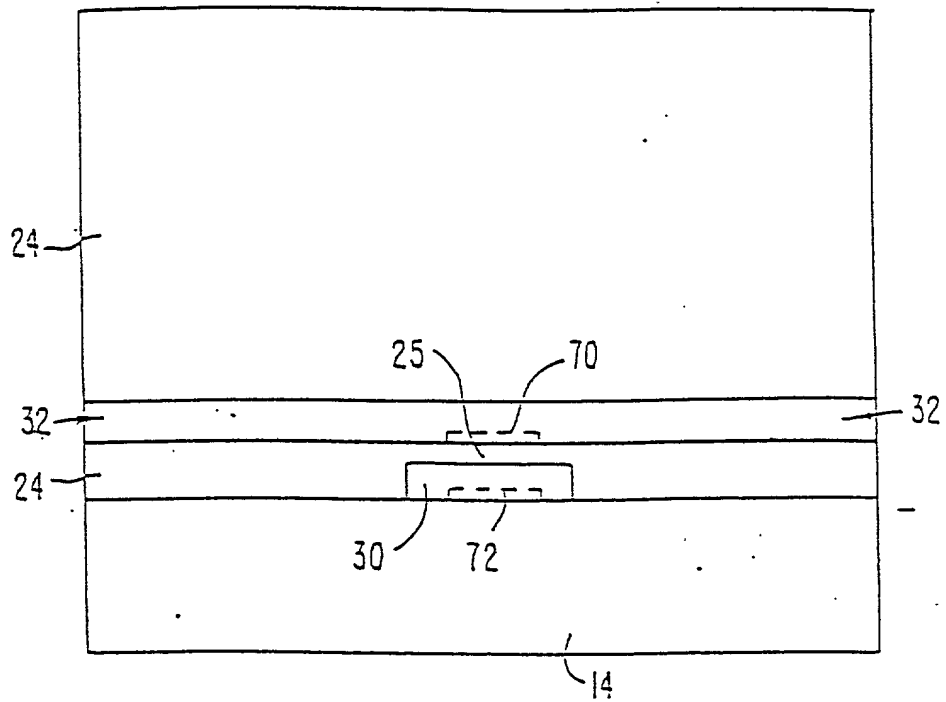


FIG. 21A

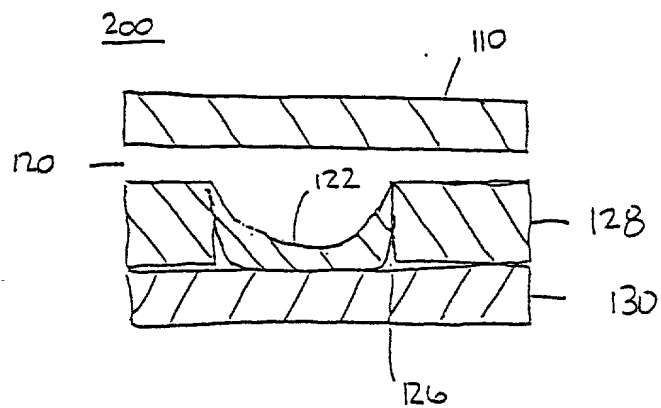


FIG. 21B

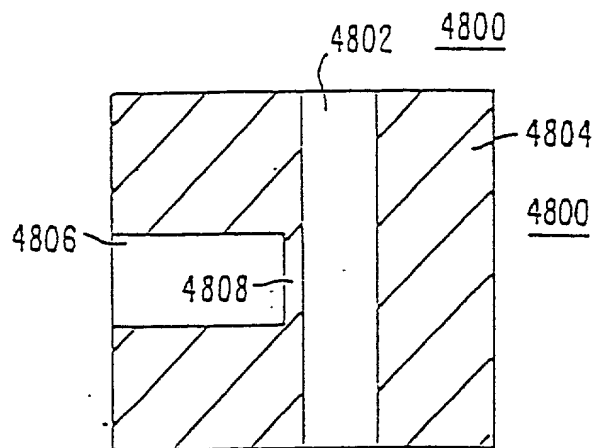


Fig 22A

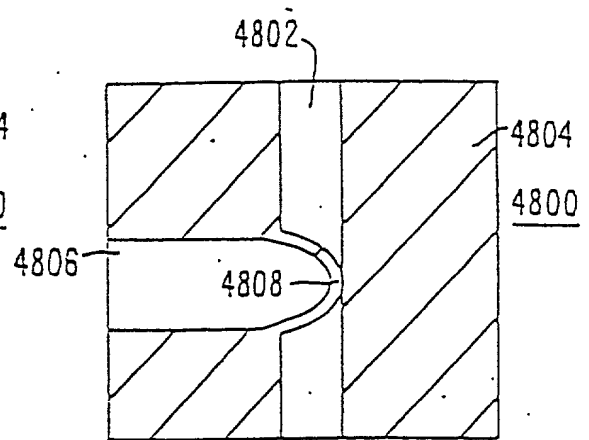
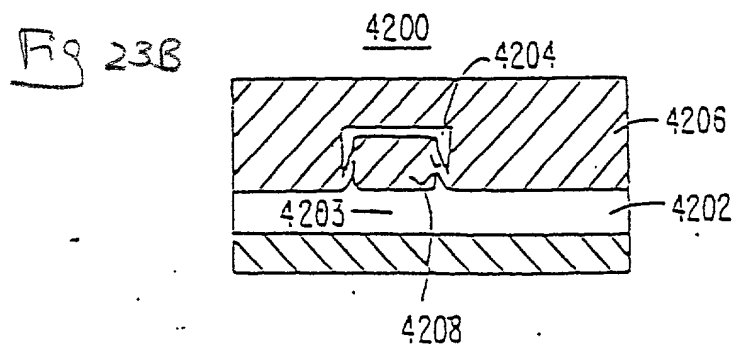
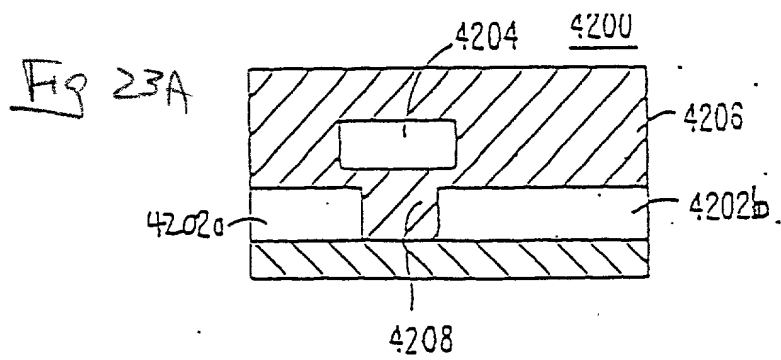


Fig 22B



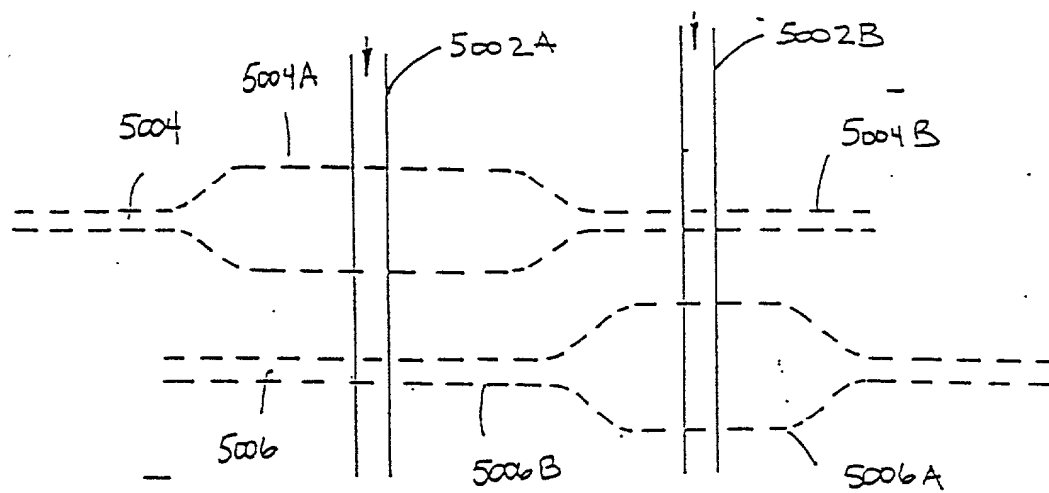


Fig 24

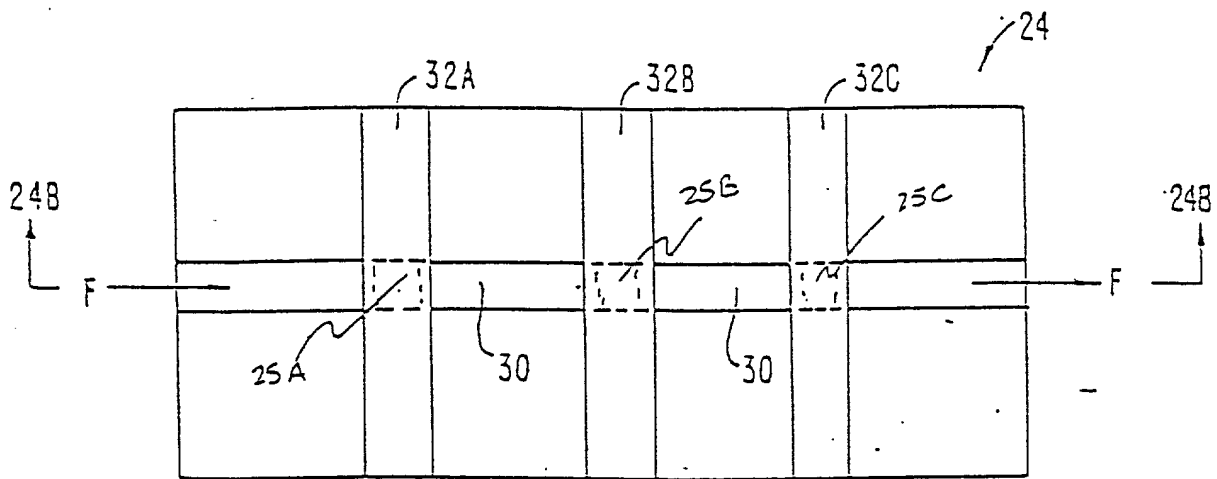


Fig 25A

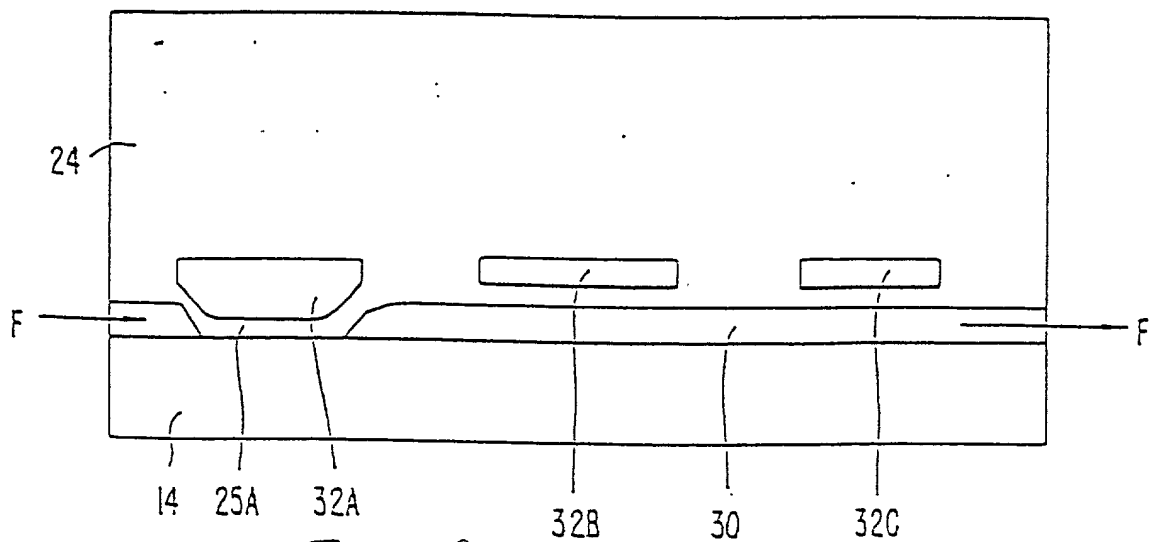


Fig 25B

